Abstracts

Multilevel Optimization of High Speed VLSI Interconnect Networks by Decomposition

Y. Wei, Q.-J. Zhang and M. Nakhla. "Multilevel Optimization of High Speed VLSI Interconnect Networks by Decomposition." 1994 Transactions on Microwave Theory and Techniques 42.9 (Sep. 1994, Part I [T-MTT]): 1638-1650.

A multilevel optimization technique is developed for large-scale and hierarchical optimization of high-speed VLSI interconnects modeled by distributed transmission lines. Mathematical programming decomposition is combined with network tearing where the overall network is optimized by a set of parallel suboptimizations. The technique takes advantage of VLSI interconnects in the hierarchy of IC, multichip modules (MCM) and printed circuit board (PCB), and is faster than standard optimization. The convergence property of the technique is derived through Gauss-Seidel relaxation analysis and optimality conditions for the multiple suboptimizations.

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